

REMARKS

Claims 1-20 are pending in the present application.

I. FORMAL MATTERS

The First Office Action does not indicate whether the formal drawings filed on November 21, 2003 are acceptable. Applicant respectfully requests the Examiner to do so.

Applicant notes with appreciation that the First Office Action acknowledges the claim to foreign priority under 35 U.S.C. § 119(a)-(d) or (f) and indicates that the certified copies of the priority documents have been received.

Applicant notes with appreciation that the Office Action includes a copy of the PTO Form 1449 that was submitted in the Information Disclosure Statement filed on

November 21, 2003. Each reference is initialed by the Examiner, thereby indicating that these references were considered and should be listed on the face of any patent that issues from the present application.

## II. PRIOR ART REJECTION

The Examiner has rejected claims 1-18 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,813,022 (Ramsey). This rejection is traversed.

The present invention is characterized by determining whether or not processing of a task is possible only with access to the cache in accordance with the amount of memory needed to process the task, and then, when it is determined that the processing is possible, inhibiting access to the external memory. That is, the CPU is arranged to control access to the external memory in accordance with the amount of memory needed to process a new task.

The present invention is also characterized in that the power supply to the external memory is stopped when access to the external memory is inhibited. That is, the CPU stops power to the external memory when the task is processed only with access to the cache.

Applicant submits that none of the cited references teaches or suggests that the amount of memory needed to process a new task is considered in the controlling access to the external memory.

The Examiner asserts that Ramsey discloses all of the elements of the rejected claims. Applicant submits that none of the cited references teaches or suggests that the power supply to the external memory is stopped when access to the external memory is inhibited. The Examiner asserts that this feature is taught in column 7, lines 58-61 of Ramsey. However, this section of Ramsey merely teaches that the L2 cache memory 208 is placed into low power mode when a stop grant acknowledge cycle is detected on

the processor bus 202. This appears to be significantly different than claim 9. Firstly, in the present invention, when access to the external memory is inhibited, power supply to the external memory is stopped. In contrast, column 7, lines 58-61 of Ramsey teaches to place the cache memory 208 in low power mode (i.e., not stopped). Secondly, in Ramsey, this low power mode is implemented when a stop grant acknowledge cycle is detected on the processor bus 202, not when processing of a task is possible only with access to the cache, as in claim 9.

Because, Ramsey does not teach or suggest these claim features, the rejection of claims 1-18 under 35 U.S.C. § 102(b) is overcome.

Applicant submits that new claims 19 and 20 are also patentable over Ramsey for at least the reasons presented above with respect to claims 1-18.

Based on the foregoing, Applicant submits that the present application is in condition for allowance and allowance is respectfully solicited. If the Examiner believes

that any of the outstanding issues could be resolved by a telephone conference,

Applicant respectfully requests the Examiner to contact the undersigned at the telephone number listed below.

Applicant believes that no additional fees are due for the subject application.

However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. 04-1105.

Respectfully Submitted,

Date: March 20, 2006  
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By: 

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